

## 1. General description

Planar passivated Silicon Controlled Rectifier with sensitive gate in a TO92 plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic ICs and other low power gate trigger circuits.

## 2. Features and benefits

- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Direct triggering from low power gate circuits and logic ICs

## 3. Applications

- Ignition circuits
- Lighting ballasts
- Protection circuits
- Switched Mode Power Supplies

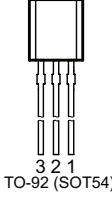

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Absolute maximum rating</b>						
$V_{RRM}$	repetitive peak reverse voltage		-	-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	0.8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25 \text{ }^\circ\text{C}$ ; $t_p = 10 \text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	8	A
		half sine wave; $T_{j(init)} = 25 \text{ }^\circ\text{C}$ ; $t_p = 8.3 \text{ ms}$	-	-	9	A
$T_j$	junction temperature		-	-	125	$^\circ\text{C}$
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12 \text{ V}$ ; $I_T = 10 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	50	200	$\mu\text{A}$
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 268 \text{ V}$ ; $T_j = 125 \text{ }^\circ\text{C}$ ; $R_{GK} = 1 \text{ k}\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	500	800	-	V/ $\mu\text{s}$
		$V_{DM} = 268 \text{ V}$ ; $T_j = 125 \text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 12</a>	-	25	-	V/ $\mu\text{s}$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 <p>TO-92 (SOT54)</p>	 <p>sym037</p>
2	G	gate		
3	K	cathode		

## 6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BT169D	TO92	BT169D,112	Bulk	1000	SOT54	14-Nov-2013
BT169D	TO92	BT169DEP	Bulk	1000	SOT54	14-Nov-2013
BT169D	TO92	BT169D,126	Reel	2000	SOT54 wide pitch	14-Nov-2013
BT169D	TO92	BT169D,116	Reel	2000	SOT54 wide pitch	14-Nov-2013
BT169D/01	TO92	BT169D/01,112	Bulk	1000	SOT54	14-Nov-2013
BT169D/DG	TO92	BT169D/DG,126	Reel	2000	SOT54 wide pitch	14-Nov-2013

## 7. Marking

Table 4. Marking codes

Type number	Marking codes
BT169D	BT169DH

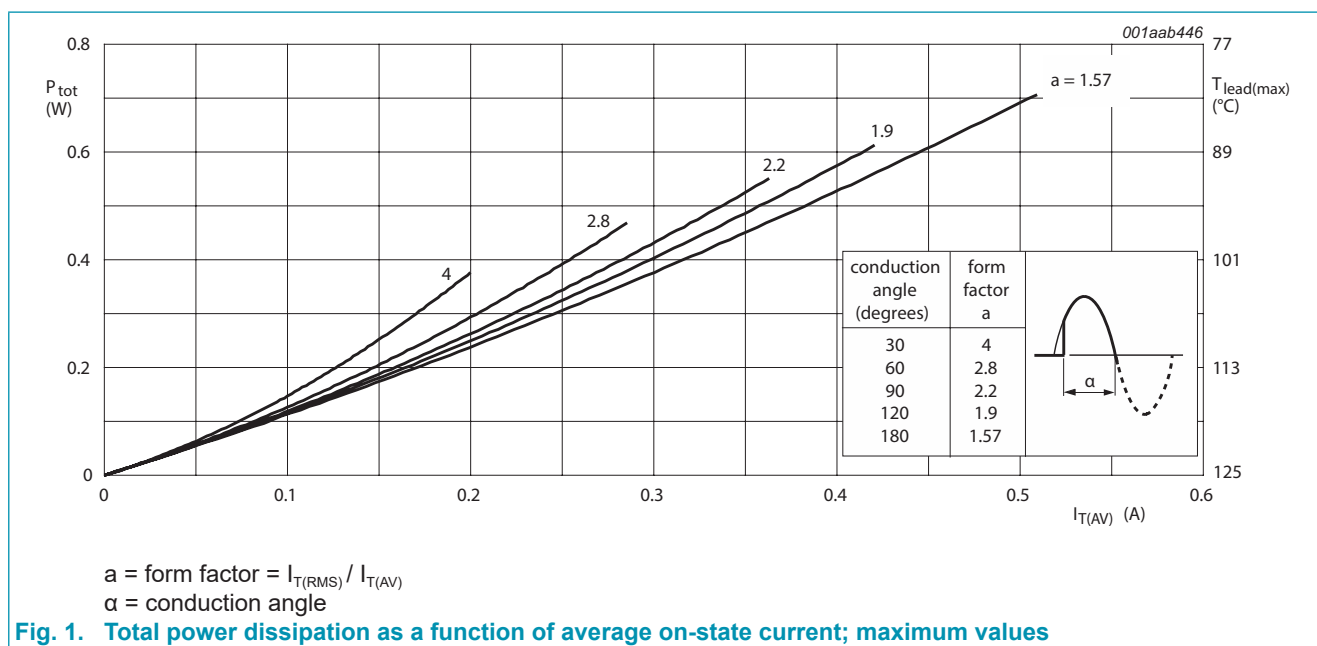
## 8. Limiting values

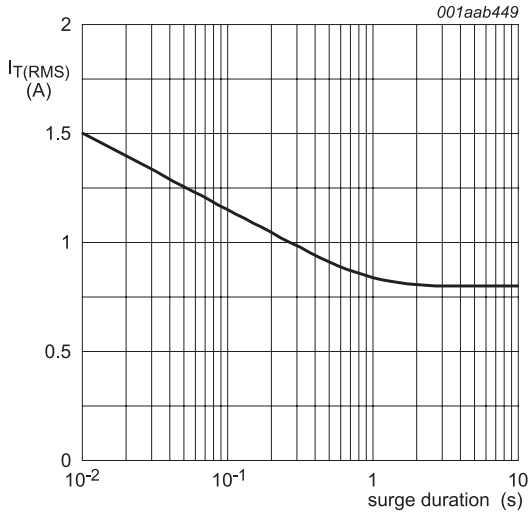
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	400	V
$V_{RRM}$	repetitive peak reverse voltage		-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$ ; Fig. 1	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$ ; Fig. 2; Fig. 3	-	0.8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 10\text{ ms}$ ; Fig. 4; Fig. 5	-	8	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 8.3\text{ ms}$	-	9	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	0.32	$\text{A}^2\text{s}$
$di_T/dt$	rate of rise of on-state current	$I_T = 2\text{ A}$ ; $I_G = 10\text{ mA}$ ; $dI_G/dt = 100\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current		-	1	A
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	150	$^{\circ}\text{C}$
$T_j$	junction temperature		[1]	125	$^{\circ}\text{C}$

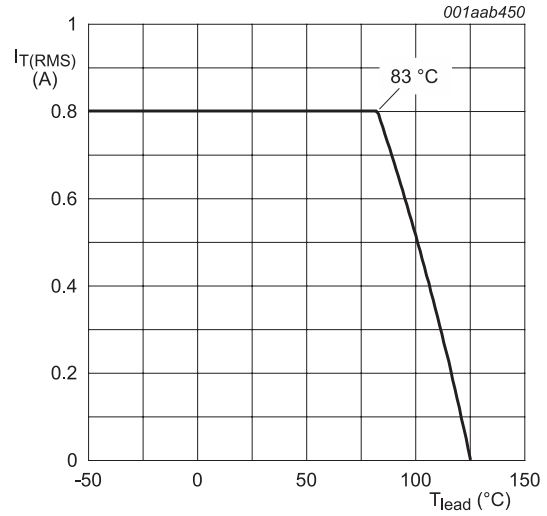
[1] Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.



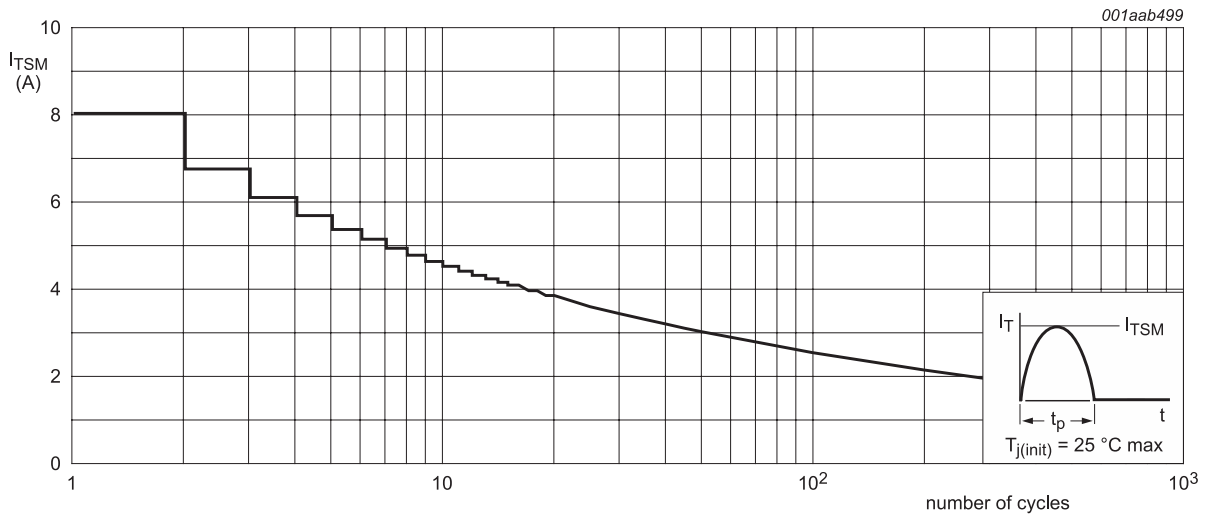


$f = 50 \text{ Hz}; T_{\text{lead}} = 83 \text{ }^\circ\text{C}$

**Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents**

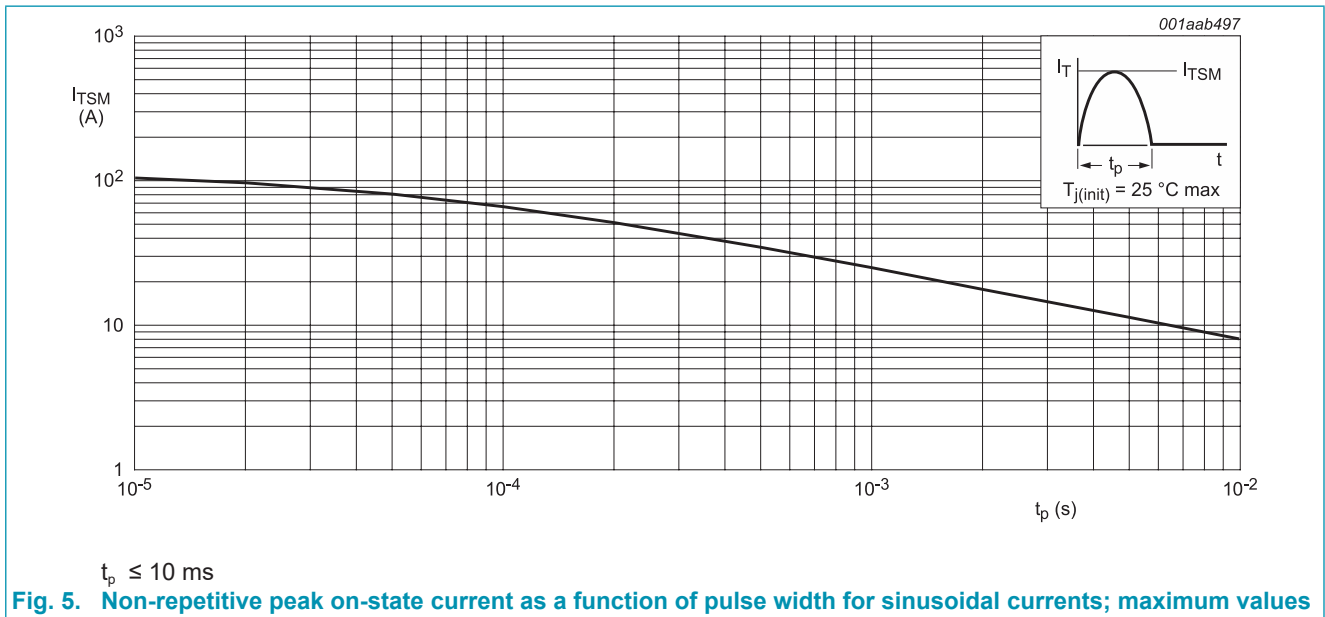


**Fig. 3. RMS on-state current as a function of lead temperature; maximum values**



$f = 50 \text{ Hz}$

**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**



## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	<a href="#">Fig. 6</a>	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W

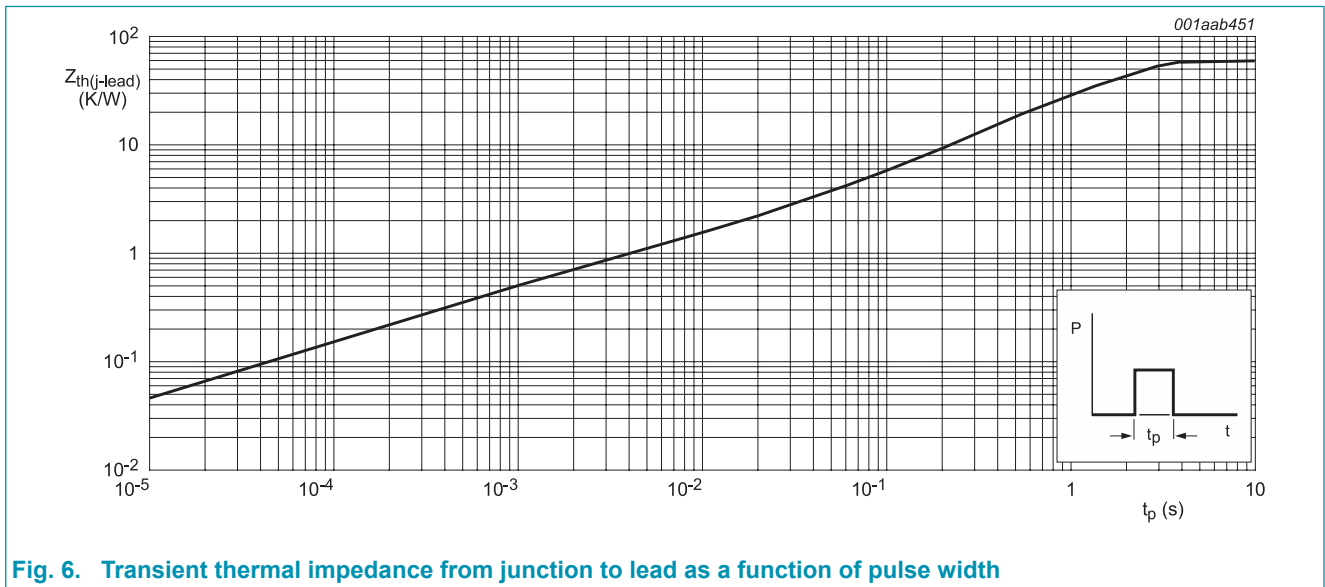


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	50	200	$\mu\text{A}$
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.5\text{ mA}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>	-	2	6	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	2	5	mA
$V_T$	on-state voltage	$I_T = 1.2\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	1.25	1.7	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	0.5	0.8	V
		$V_D = 400\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 125\text{ °C}$	0.2	0.3	-	V
$I_D$	off-state current	$V_D = 400\text{ V}$ ; $T_j = 125\text{ °C}$	-	0.05	0.1	mA
$I_R$	reverse current	$V_R = 400\text{ V}$ ; $T_j = 125\text{ °C}$	-	0.05	0.1	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 268\text{ V}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 1\text{ k}\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	500	800	-	$\text{V}/\mu\text{s}$
		$V_{DM} = 268\text{ V}$ ; $T_j = 125\text{ °C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit; <a href="#">Fig. 12</a>	-	25	-	$\text{V}/\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 2\text{ A}$ ; $V_D = 400\text{ V}$ ; $I_G = 10\text{ mA}$ ; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$ ; $T_j = 25\text{ °C}$	-	2	-	$\mu\text{s}$
$t_q$	commutated turn-off time	$V_{DM} = 268\text{ V}$ ; $T_j = 125\text{ °C}$ ; $I_{TM} = 1.6\text{ A}$ ; $V_R = 35\text{ V}$ ; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$ ; $dV_D/dt = 2\text{ V}/\mu\text{s}$ ; $R_{GK(ext)} = 1\text{ k}\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ )	-	100	-	$\mu\text{s}$

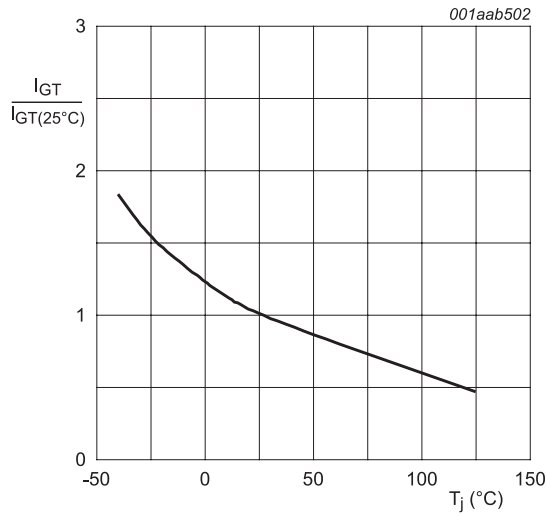
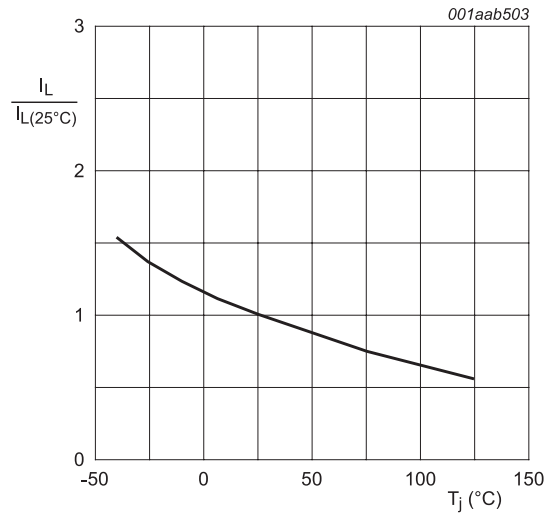
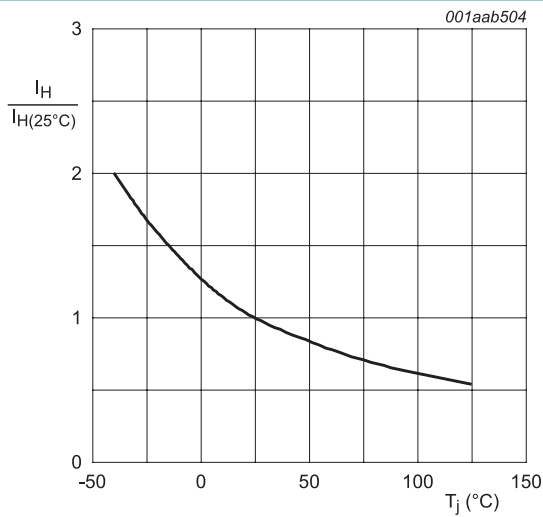


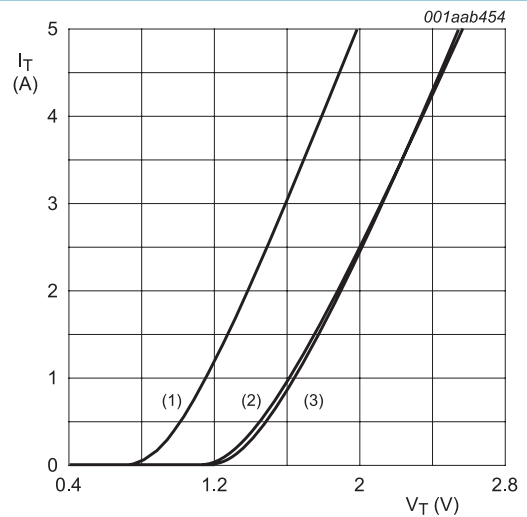
Fig. 7. Normalized gate trigger current as a function of junction temperature



$R_{GK} = 1 \text{ k}\Omega$   
Fig. 8. Normalized latching current as a function of junction temperature



$R_{GK} = 1 \text{ k}\Omega$   
Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.067 \text{ V}; R_s = 0.187 \Omega$   
(1)  $T_j = 125^\circ\text{C}$ ; typical values  
(2)  $T_j = 125^\circ\text{C}$ ; maximum values  
(3)  $T_j = 25^\circ\text{C}$ ; maximum values  
Fig. 10. On-state current as a function of on-state voltage



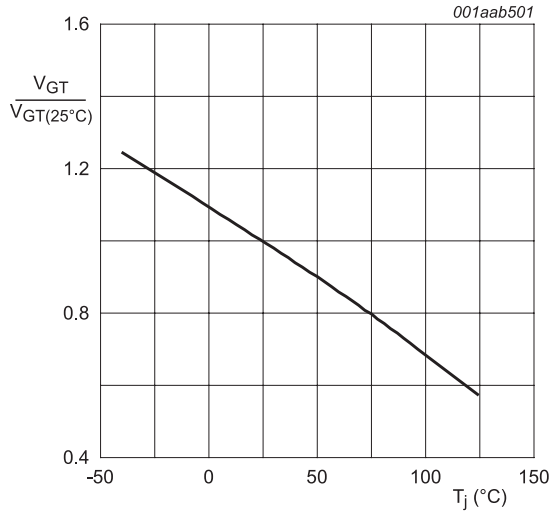
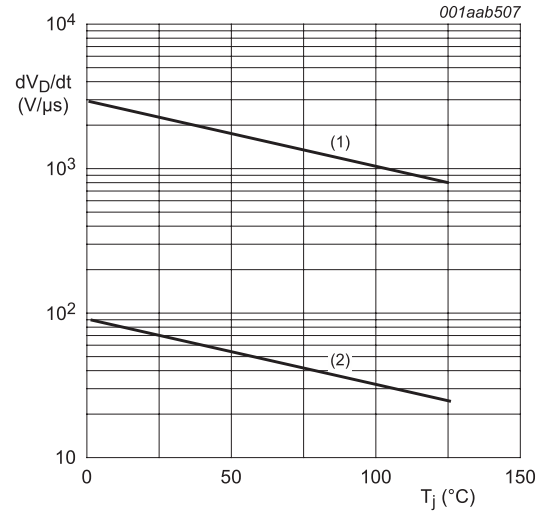


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

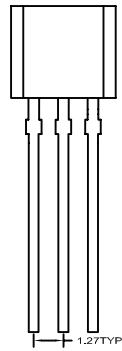


(1)  $R_{GK} = 1 \text{ k}\Omega$ ;  
 (2) gate open circuit

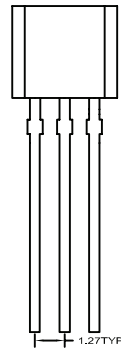
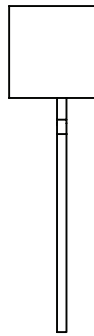
Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

## 11. Package outline

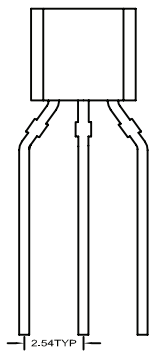
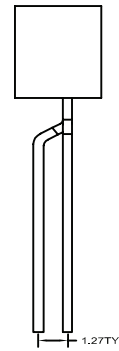
### SOT54 PACKAGE OUTLINE



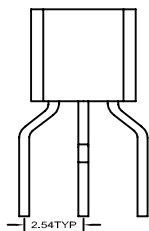
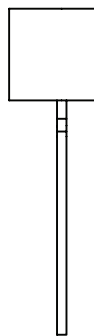
SOT54  
Bulk Pack - 412



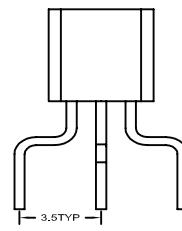
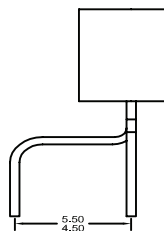
SOT54 LEADS ON CIRCLE  
Bulk Pack - 112



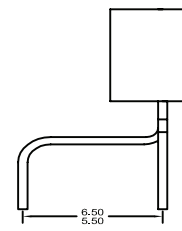
SOT54 WIDE PITCH  
Tape/ Reel Pack - 116  
Ammo Pack - 126



SOT54 LEAD BEND L01  
Bulk Pack - 412



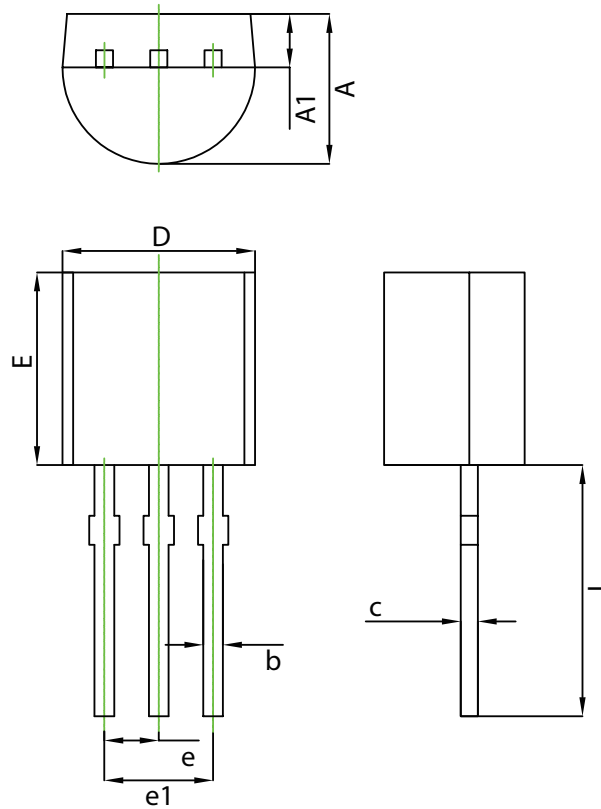
SOT54 LEAD BEND L02  
Bulk Pack - 412



Remark: Detailed dimensions refer to POD drawing.

Plastic single-ended leaded(through hole) package; 3 leads

TO92



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.300	3.700	0.130	0.146
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	4.300	4.700	0.169	0.185
E	4.300	4.700	0.169	0.185
e	1.270 TYP.		0.050 TYP.	
e1	2.440	2.640	0.096	0.104
L	14.100	14.500	0.555	0.571

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 26 October 2022

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