

## 1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a TO220F "full pack" plastic package intended for use in applications requiring good bidirectional blocking voltage and high current surge capability with high thermal cycling performance and high junction temperature capability ( $T_{j(max)} = 150\text{ °C}$ ).

## 2. Features and benefits

- High junction operating temperature capability ( $T_{j(max)} = 150\text{ °C}$ )
- Good bidirectional blocking voltage capability
- High current surge capability
- High thermal cycling performance
- Isolated mounting base package
- Planar passivated for voltage ruggedness and reliability

## 3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation
- High junction operating temperature capability ( $T_{j(max)} = 150\text{ °C}$ )

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Values	Unit
<b>Absolute maximum rating</b>				
$V_{RRM}$	repetitive peak reverse voltage		650	V
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 94\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	12	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	120	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 8.3\text{ ms}$	132	A
$T_j$	junction temperature		150	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	-	5	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>	-	7	20	mA
$V_T$	on-state voltage	$I_T = 12\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	1.18	1.54	V
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 436\text{ V}$ ; $T_j = 150\text{ °C}$ ; $R_{GK} = 100\ \Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform;	200	1000	-	V/ $\mu$ s

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		
2	A	anode		
3	G	gate		
mb	n.c.	mounting base; isolated		

## 6. Ordering information

Table 3. Ordering information

Type number	Package name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BT151X-650LT	TO220F	BT151X-650LTQ	Tube	50	SOT186A	14-Nov-2013

## 7. Marking

Table 4. Marking codes

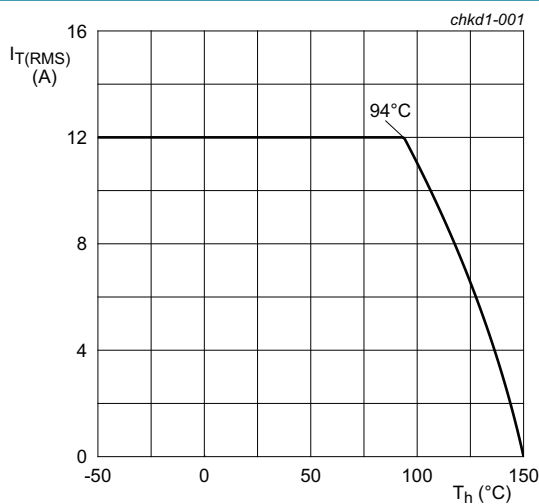
Type number	Marking codes	
	Assembly factory: d	Assembly factory: A
BT151X-650LT	BT151X 650LT PJdxxxx xx	BT151X 650LT PJAxxxx xx

## 8. Limiting values

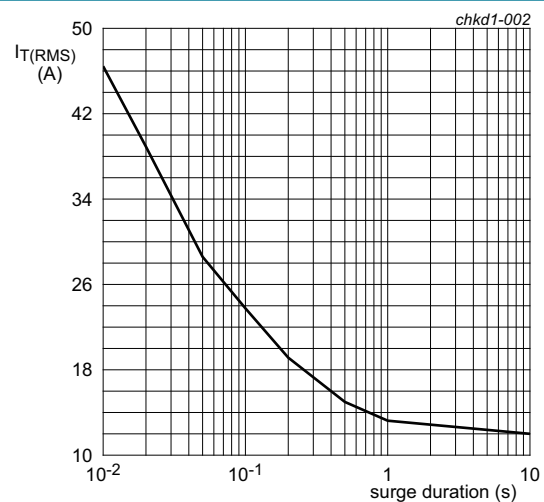
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

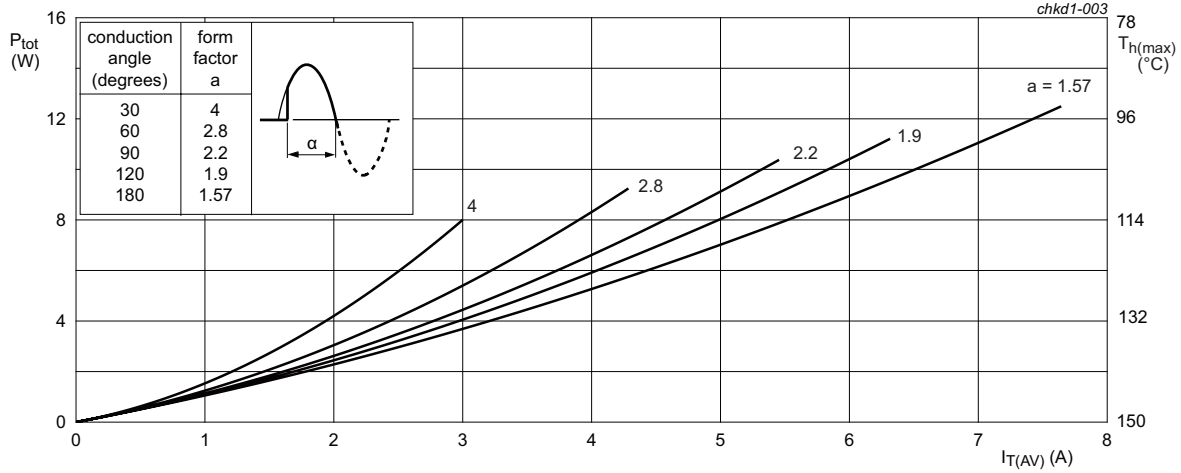
Symbol	Parameter	Conditions	Values	Unit
$V_{DRM}$	repetitive peak off-state voltage		650	V
$V_{RRM}$	repetitive peak reverse voltage		650	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_h \leq 94\text{ }^\circ\text{C}$	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_h \leq 94\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	12	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	120	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$ ; $t_p = 8.3\text{ ms}$	132	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ms}$ ; sine wave	72	$\text{A}^2\text{s}$
$di_T/dt$	rate of rise of on-state current	$I_G = 10\text{mA}$	50	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current		2	A
$V_{RGM}$	peak reverse gate voltage		5	V
$P_{GM}$	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.5	W
$T_{stg}$	storage temperature		-40 to 150	$^\circ\text{C}$
$T_j$	junction temperature		150	$^\circ\text{C}$



**Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values**

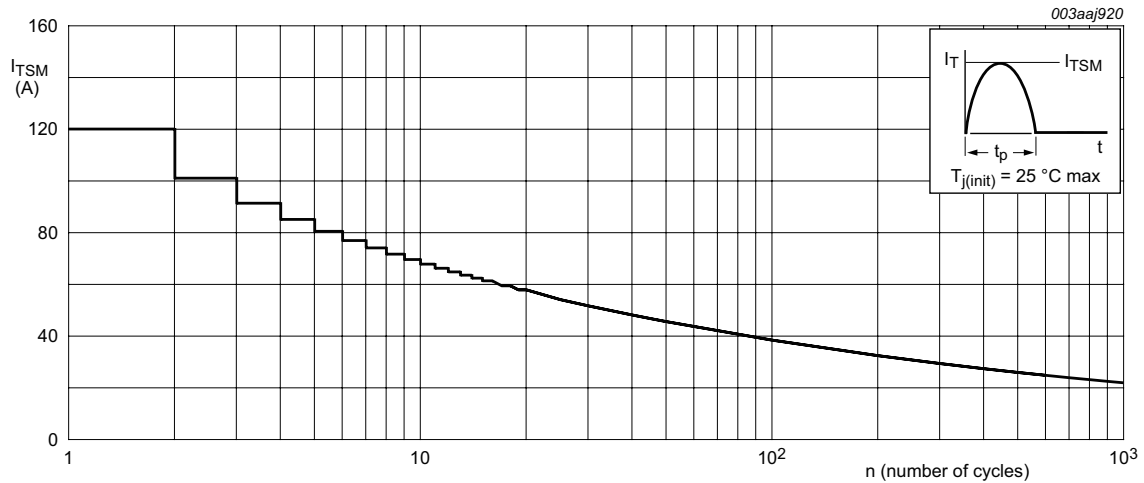


**Fig. 2. RMS on-state current as a function of surge duration; maximum values**  
 $f = 50\text{ Hz}$ ;  $T_h = 94\text{ }^\circ\text{C}$



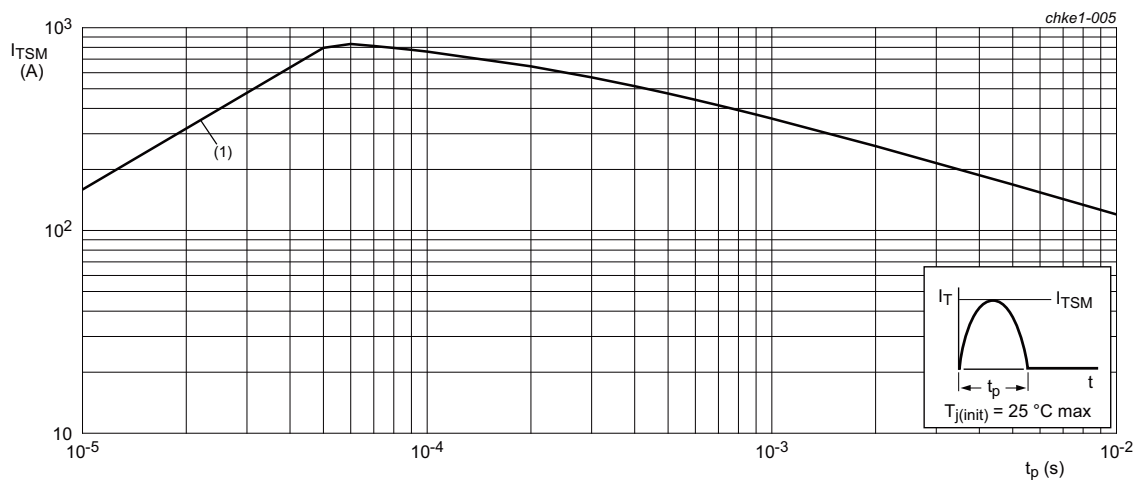
$\alpha$  = conduction angle  
 $a$  = form factor =  $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of average on-state current; maximum values



$f = 50$  Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$  ms ;  
 (1)  $di_T/dt$  limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 6	-	-	4.5	K/W
		without heatsink compound; Fig. 6	-	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W

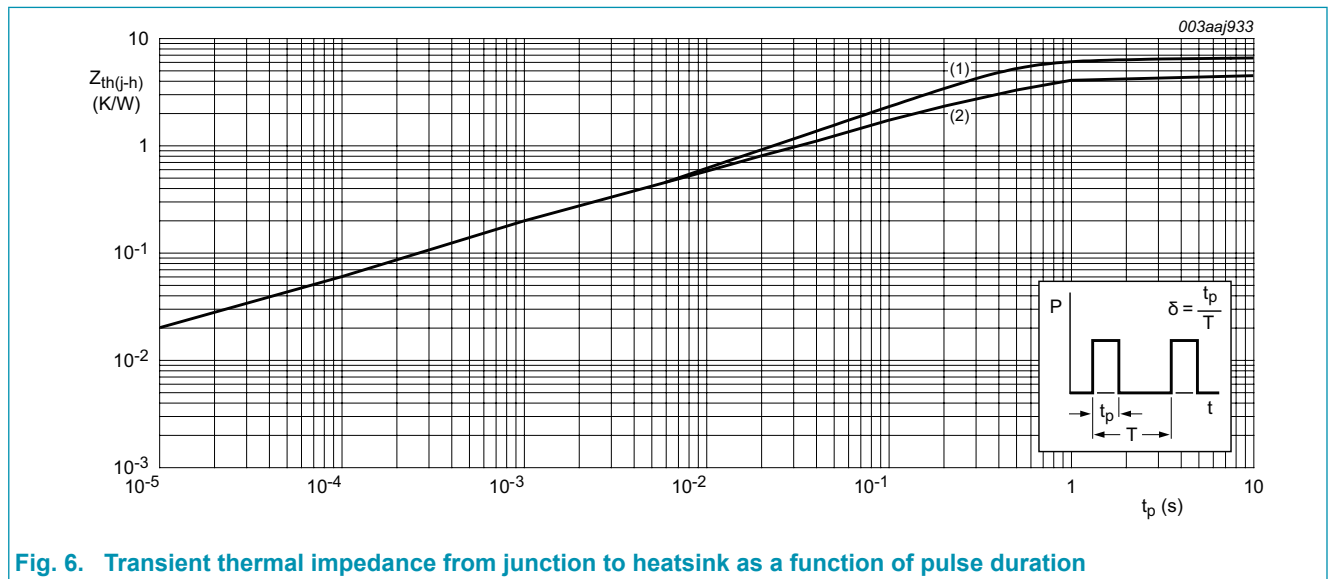


Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse duration

## 10. Isolation characteristics

Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz $\leq$ f $\leq$ 60 Hz; RH $\leq$ 65 %; from all pins to external heatsink; sinusoidal waveform; clean and dust free	-	-	2500	V
$C_{isol}$	isolation capacitance	from cathode to external heatsink	-	10	-	pF

## 11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 7	-	-	5	mA
$I_L$	latching current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 8	-	10	40	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 9	-	7	20	mA
$V_T$	on-state voltage	$I_T = 12\text{ A}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 10	-	1.18	1.54	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 11	-	0.6	1	V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 150\text{ }^\circ\text{C}$	0.2	0.4	-	V
$I_D$	off-state current	$V_D = 650\text{ V}; T_j = 150\text{ }^\circ\text{C}$	-	-	1	mA
$I_R$	reverse current	$V_D = 650\text{ V}; T_j = 150\text{ }^\circ\text{C}$	-	-	1	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 436\text{ V}; T_j = 150\text{ }^\circ\text{C}; R_{GK} = 100\text{ }\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform;	200	1000	-	V/ $\mu\text{s}$
		$V_{DM} = 436\text{ V}; T_j = 150\text{ }^\circ\text{C}; (V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit	50	-	-	V/ $\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 12\text{ A}; V_D = 650\text{ V}; I_G = 10\text{ mA}$ ; $(dI_G/dt)_M = 5\text{ A}/\mu\text{s}; T_j = 25\text{ }^\circ\text{C}$	-	2	-	$\mu\text{s}$
$t_q$	commutated turn-off time	$V_{DM} = 436\text{ V}; T_j = 150\text{ }^\circ\text{C}; I_{TM} = 12\text{ A}; V_R = 25\text{ V}; dV_D/dt = 30\text{ V}/\mu\text{s}; (dI_T/dt)_M = 30\text{ A}/\mu\text{s}; R_{GK(ext)} = 100\text{ }\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ )	-	70	-	$\mu\text{s}$

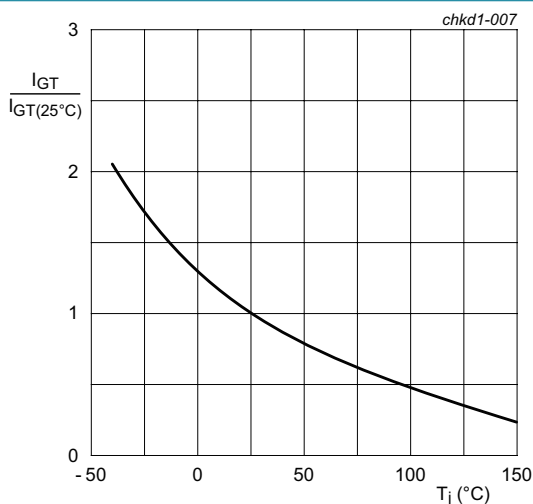


Fig. 7. Normalized gate trigger current as a function of junction temperature

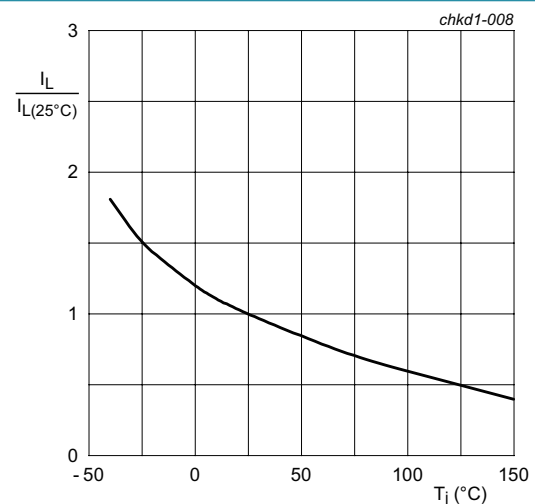


Fig. 8. Normalized latching current as a function of junction temperature

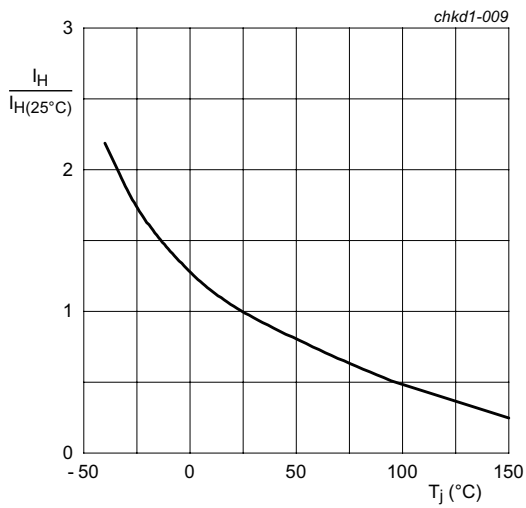
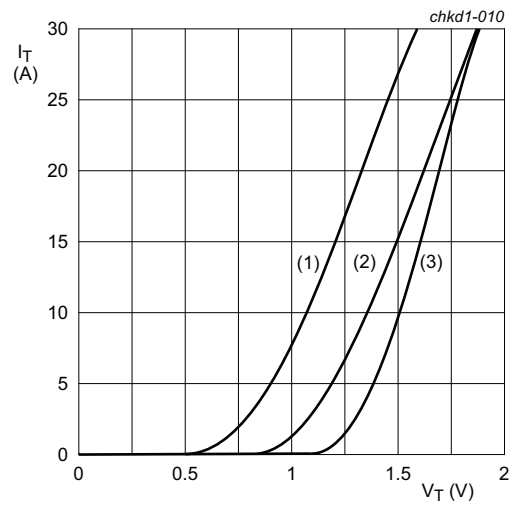


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 0.967 \text{ V}; R_s = 0.0354 \ \Omega$   
 (1)  $T_j = 150 \ ^\circ\text{C}$ ; typical values  
 (2)  $T_j = 150 \ ^\circ\text{C}$ ; maximum values  
 (3)  $T_j = 25 \ ^\circ\text{C}$ ; maximum values

Fig. 10. On-state current as a function of on-state voltage

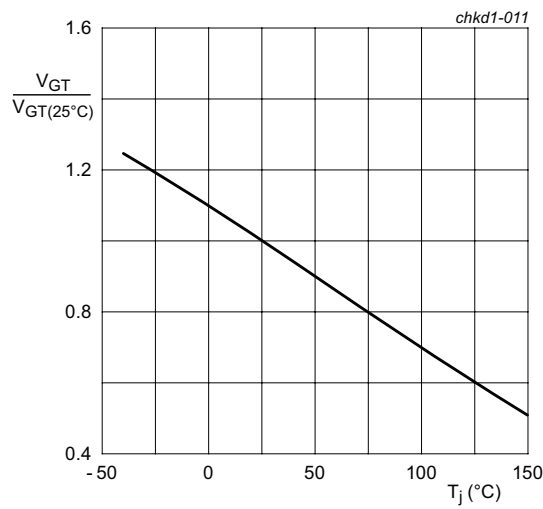


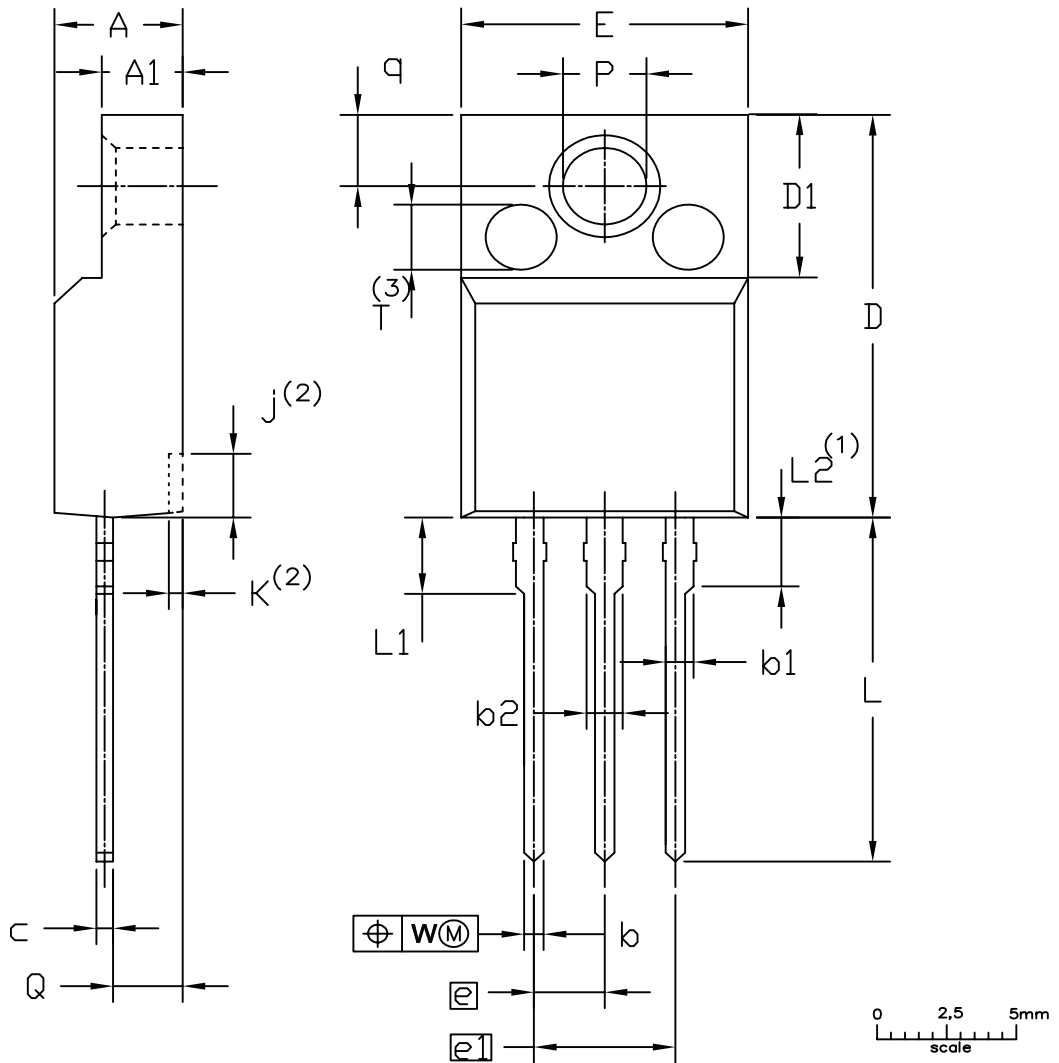
Fig. 11. Normalized gate trigger voltage as a function of junction temperature

## 12. Package outline

Assembly factory: d & A

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"

SOT186A



UNIT	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D	D <sub>1</sub>	E	e	e <sub>1</sub>	j <sup>(2)</sup>	k <sup>(2)</sup>	L	L <sub>1</sub>	L <sub>2</sub> <sup>(1)</sup> max.	P	Q	q	W	T <sup>(3)</sup>
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3			2.7	0.6	14.4	3.30		3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7	2.54	5.08	1.7	0.4	13.5	2.79	3	3.0	2.3	2.6		

**Notes**

1. Terminal dimensions within this zone are uncontrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT186A		3 LEADS TO220F			2013-11-14



## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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